IN THE SPECIFICATION:

Please replace the section of the specification entitled Summary Of The Invention starting on page 3, line 25, and continuing through page 8, line 21, with the following text:

"SUMMARY OF THE INVENTION

B1

In accordance with the present invention, a semiconductor device that has a wiring pattern that is formed by etching a conductive layer using a resist pattern as a mask includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation, and

a second wiring having a connection region to be connected to the contact section,

wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section, and

the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring.

In the semiconductor device in accordance with the present invention, since the extension section is provided in the connection region to be connected to the contact section, the connection region of the wiring can almost completely cover the contact section in the lower layer. Therefore, the contact resistance between the contact section formed in the connection hole (contact hole or via hole) and the wiring can be made small, the wiring reliability can be improved.

A variety of embodiments may be provided for the semiconductor device of the present invention as described below. These embodiments are applicable to semiconductor devices having structures to be described below.

B1 Cont.

(a) The separation is shorter than a specified separation and there is a minimum separation between wirings in a wiring pattern (hereafter referred to as a "minimum inter-wiring separation"). The minimum inter-wiring separation may vary depending on the design rules, and may be, for example, 0.1 μm or greater but 1 μm or smaller.

(b) The connection region is square in its plan configuration having dimensions that are greater than or equal to dimensions of the contact section.

(c) The extension section may preferably have the same width as the width of the wiring, and may preferably have the same extension length as the width of the wiring. Also, the extension section may preferably be square in its plan configuration.

Furthermore, semiconductor device in accordance with the present invention can have the following structures.

(1) A semiconductor device includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and extending in parallel with the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(2) A semiconductor device includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(3) A semiconductor device includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and having a section extending in parallel with the first wiring and a section extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(4) A semiconductor device includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having only a connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

B1 cont.

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(5) A semiconductor device includes

a contact section formed in an interlayer dielectric layer,

a plurality of first wirings formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having at least one connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the plurality of first wirings.

(6) A semiconductor device includes

a contact section formed in an interlayer dielectric layer, and

a wiring having a connection region to be connected to the contact section,

wherein the connection region of the wiring has a generally square plan configuration, and

B1 Concl'd

the wiring has an extension section extending in a non-wiring region in the connection region."

Please replace the heading on page 1, line 11, with the following text:

B2 "BACKGROUND OF THE INVENTION"

Please replace the heading on page 10, lines 8-9, with the following text:

B3 "DETAILED DESCRIPTION OF THE INVENTION"

Please replace the paragraph on page 13, lines 22-29, with the following text:

B4 "In the example shown in the figure, a first wiring 17 is disposed separated from the contact sections 36 and 46 by a separation shorter than a specified separation (about a minimum inter-wiring separation in this example). A second wiring 15 and the third wiring 16 are disposed in proximity to the first wiring 17. The first and second wirings 17 and 15 both extend in the X direction, and a third wiring 16 extends in the Y direction. Also, the second and third wirings 15 and 16 are disposed separated from the first wiring 17 by a minimum inter-wiring separation."

Please replace the paragraph on page 17, lines 21-30,with the following text:

B5 "In the example shown in the figure, a first wiring 17 is disposed separated from the contact sections 36 and 46 by a separation shorter than a specified separation (about a minimum inter-wiring separation in this example). A second wiring 31 and a third wiring 32 are disposed in proximity to the first wiring 17. The first wiring 17 extends in the X direction, and the second wiring 31 extends in the X direction and the Y direction. The third wiring 32 is composed only of a contact region for connecting upper and lower contact sections. Also, the second and third

B5 (concl'd) wirings 31 and 32 are disposed separated from the first wiring 17 by a minimum inter-wiring separation."

Please replace the section of the specification entitled Abstract on page 33, lines 1-12, with the following text:

"ABSTRACT

B6 A semiconductor device has a wiring pattern formed by etching a conductive layer using a resist pattern as a mask. The semiconductor device includes a contact section and a wiring. The contact section is formed in an interlayer dielectric layer. The wiring has a connection region to be connected to the contact section. The connection region of the wiring has a generally square plan configuration. The wiring has an extension section extending in a non-wiring region in the connection region."

IN THE CLAIMS:

Please replace the text of claims 2-8, 13, and 14 with the following text:

B7 2. (Amended) The semiconductor device according to claim 1, wherein the separation is shorter than a specified separation and there is a minimum separation between wirings in the wiring pattern.

3. (Amended) The semiconductor device according to claim 1, wherein the connection region is square in its plan configuration having dimensions that are greater than or equal to dimensions of the contact section.

4. (Amended) The semiconductor device according to claim 1, wherein the extension section has an identical width as a width of the wiring.